

Claims

What is claimed is:

- 5 1. A method for fabricating a semiconductor device comprising:
forming a gate wire over a gate insulating layer on a predetermined portion of an
active region of a first conductivity-type semiconductor substrate;
forming source/drain regions in the substrate at opposite edges of the gate wire by
selectively ion-implanting a high density of a second conductivity-type impurity;
10 forming a second conductivity-type junction diode in the substrate at a
predetermined distance apart from the source/drain regions;
forming an inter-level insulating layer having a plurality of contact holes to expose
predetermined portions of the gate wire and junction diode;
forming conductivity plugs in the contact holes;
15 forming a metal layer on the inter-level insulating layer; and
simultaneously forming a metal wire coupled to the gate wire, and a dummy metal
pattern coupled to the junction diode by selectively etching the metal layer to expose
predetermined portions of the surface of the inter-level insulating layer.
- 20 2. The method, as defined in claim 1, wherein the metal wire and junction diode
comprise Al alloy or Cu alloy.
3. The method, as defined in claim 1, wherein the dummy metal pattern is formed in
a linear strip or double-folded shape.

4. The method, as defined in claim 1, wherein the metal wire and the dummy metal pattern are oriented to be substantially parallel.

5. The method, as defined in claim 1, wherein the dummy metal pattern is shorter than the metal wire.

6. The method, as defined in claim 1, wherein the metal wire and the dummy metal pattern are formed to be spaced apart at a distance of less than 2 micrometers.

7. A method for fabricating a semiconductor device comprising:
sequentially forming first and second conductivity-type wells in a semiconductor substrate;

forming a gate wire over a gate insulating layer on a predetermined portion of the first conductivity-type well;

forming source/drain regions in the first conductivity well at opposite edges of the gate wire by selectively ion implanting a high density of a second conductivity-type impurity in the first conductivity-type well;

forming a second conductivity-type first junction diode in the first conductivity-type well at a predetermined distance apart from the source/drain regions;

forming a first conductivity-type second junction diode in the second conductivity-type well at a predetermined distance from the first junction diode;

forming a second junction diode formed in the second conductivity well at a predetermined distance apart from the first junction diode by selectively ion-implanting a

high density of first conductivity-type impurity in the second conductivity-type well;

forming an inter-level insulating layer over the gate wire and the first and second junction diodes, the inter-level insulating layer including a plurality of contact holes to expose predetermined portions of the gate wire and first and second diodes;

5 forming conductivity plugs in the contact holes;

forming a metal layer on the inter-level insulating layer;

simultaneously forming a metal wire coupled to the gate wire, and a dummy metal pattern coupled to the first and second junction diodes by selectively etching the metal layer to expose predetermined portions of the surface of the inter-level insulating layer.

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8. The method, as defined in claim 7, wherein the metal wire and junction diode comprise Al alloy or Cu alloy.

9. The method, as defined in claim 7, wherein the dummy metal pattern is formed in
15 a multi-angular shape.

10. The method, as defined in claim 7, wherein the metal wire and the dummy metal pattern are in longitudinal parallel on the inter-level insulating layer.

20 11. The method, as defined in claim 7, wherein the dummy metal pattern is shorter in length than the metal wire.

12. The method, as defined in claim 7, wherein the metal wire and the dummy metal pattern are spaced apart a distance of less than 2 micrometers.